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CONTENTS

Fault-tolerant Synchronous FSM Network Design for Path Delay Faults[1]

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Abstract

The use of modern high-speed electronic devices in high-tech industries requires high reliability of these devices. External factors such as radiation, high temperature, etc., often lead to the appearance of so-called soft faults of transient or intermittent. Such faults do not cause irrevocable changes in the equipment, and their manifestation lasts a limited time, not more than one clock cycle as a rule. Nevertheless it can affect the correct operation of the device. The accumulation of even small delays of gates in high-speed circuit along the path from the circuit input to the output can lead to an incorrect output signal. Such faults are called path delay faults. In this paper, we propose a method of fault-tolerant FSM network design for path delay faults, based on the use of a self-checking FSM network and a FSM network that implements the basic functionality without additional properties.

1. Introduction

In modern space, military, medical and etc. industries the requirements for the reliability of hardware are increased. Continuous improvements in CMOS technology, included in the nanometer scale, led to quantum mechanical effects, creating many technological problems for further scaling of CMOS devices. Nano-scale devices are limited to higher defect coefficients and increased susceptibility to soft errors (intermittent or transient).

A high level of circuit integration, high-frequency operation and low voltage in high-performance integrated circuits can occur wrongful delays. They cannot always be detected with use of the classical model of stuck-at faults. A path delay fault model (PDF) is one of the most common and useful delay models in practice [1]. In this model, it is taken into account that small delays of gates during the path and connections between them can accumulate and summarized delay may exceed the permissible level for the entire circuit. This courses to incorrect operation of the circuit.

The triple modular redundancy (TMR) [2] is one of the most common methods of providing fault tolerance. The main idea of TMR is to combine tree identical copies of the circuit and by majority vote determine the output of the system. The main difficulties in TMR are the voters (if the voter fails, the full system does not work) and high overhead.

The authors in [3] propose a method of fault tolerance for sequential circuits based on finite states machine (FSM). This method involves the addition of redundant equivalent states to protect states with a high probability of occurrence. The added states ensure that all single errors appearing in the high-state state variables or their combinational logic are protected. Tolerance for all single faults in the state variables of high frequency states or in their combinational logic is guaranteed by the added states.

Various options of fault-tolerant systems based on two replicas of the self-checking circuit [4]–[7] is proposed in [8]–[15].

In the papers [13]–[15], design of fault-tolerant circuits (combinational or sequential) based on self-checking module and unprotected for stuck-at faults and path delay faults with low overhead in comparison with architectures suggested in [10], [12] are considered.

We offer a new fault-tolerant architecture for synchronous FSM networks, in which there are two blocks: a self-checking FSM network and the usual one without additional properties. Single PDFs are considered, the duration of which does not exceed one clock cycle. A modification of self-checking FSM network for PDFs proposed in [16] is used. This approach allows to reduce hardware overhead due to the fact that in the self-checking FSM network only the

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output FSMs are observed, which allows reducing the number of checkers, and reduces expenses on the entire fault-tolerant architecture.

This paper is structured as follows. In Section 2 the self-checking synchronous FSM network for path delay faults is described. Section 3 gives the fault-tolerant synchronous FSM network design. Finally, conclusions are drawn in Section 4.

2. Self-checking Synchronous FSM Network Design

In [16] a technique for self-checking synchronous FSM network design for PDFs is proposed. Checkers only observe FSM outputs, whose output lines are simultaneously the output lines of the network as a whole. Delays in single paths from the inputs to the outputs of each FSM are considered. Monotonous implementation of FSM allows multilevel or factorized logic synthesis. Both of them provide a unidirectional manifestation of PDFs on the output lines of the corresponding FSM. The monotonous implementation is derived from the FSM description in the form of State Transition Graph (STG) using the *m*-out-of-*n* code of its states and the minor expansion of the STG products.

For an arbitrary FSM network N with *r* component to obtain the following self-checking synchronous FSM network N^S (Fig. 1).

The additional parity output (po_i) for each FSM prevents a bidirectional propagation of PDFs through the next state outputs. The presence of an additional output is only necessary if it is allowed that the fault lasts more than one clock cycle. Since if the fault has manifested itself at the outputs of the combination part of FSM corresponding to the feedback lines, then the presence of this fault by 2, 3, etc. cycles can lead to bidirectional changes of outputs even for monotonous implementation of FSM. Therefore, this manifestation will be immediately detected by an additional output. If we assume that the duration of the fault is not more than one cycle, then it is possible to implement without an additional output with preservation of the self-checking property.

This architecture allows to reduce hardware redundancy in comparison with the implementation of the network of self-checking FSMs due to the fact that checkers are used only for FSM outputs, whose output lines are simultaneously the output lines of the network as a whole.

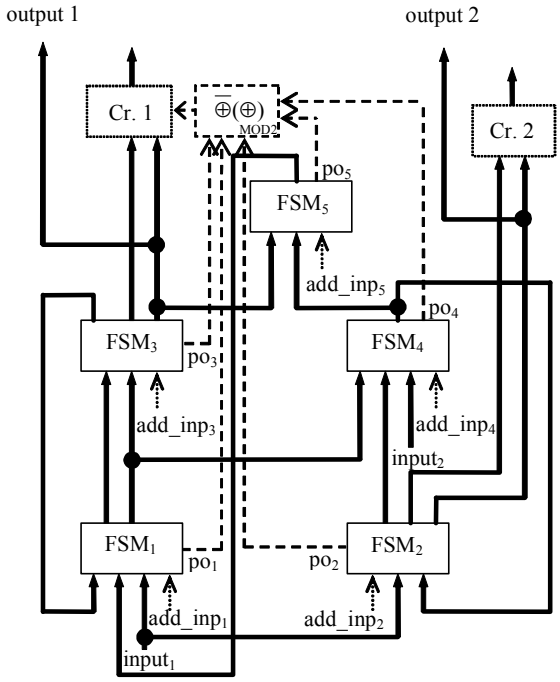

Figure 1. Self-checking synchronous FSM network

3. Fault-tolerant Synchronous FSM Network Design

The architecture of the fault-tolerant synchronous FSM network based on the architecture [15] is suggested (Fig. 2). Within this architecture, three basic blocks can be distinguished: **FSM-Net**, **SC-FSM-Net** and **MUX**. It is only possible to malfunction one unit at a time. The impact of a fault is limited to one clock cycle of the network working.

FSM-Net is a synchronous FSM network that embodies the basic functionality, each component of this block can have an arbitrary implementation. The outputs **output$_1$''** and **output$_2$''** are supplied to the input of the multiplexer (**MUX**). Arbitrary faults that change the output signals of the **FSM-Net** are admissible.

SC-FSM-Net is a self-checking synchronous FSM network constructed in accordance with the method [17]. In this architecture only the outputs of such network components are observed whose outputs are the outputs of the network as a whole. We call them output FSMs. Let l is a number of output FSMS. Inspection of these outputs is carried out by checkers of one of the unordered codes. For example, by checkers of constant-weight codes (**Checker$_1$**, **Checker$_2$**). The outputs of all checkers are connected to the input of the

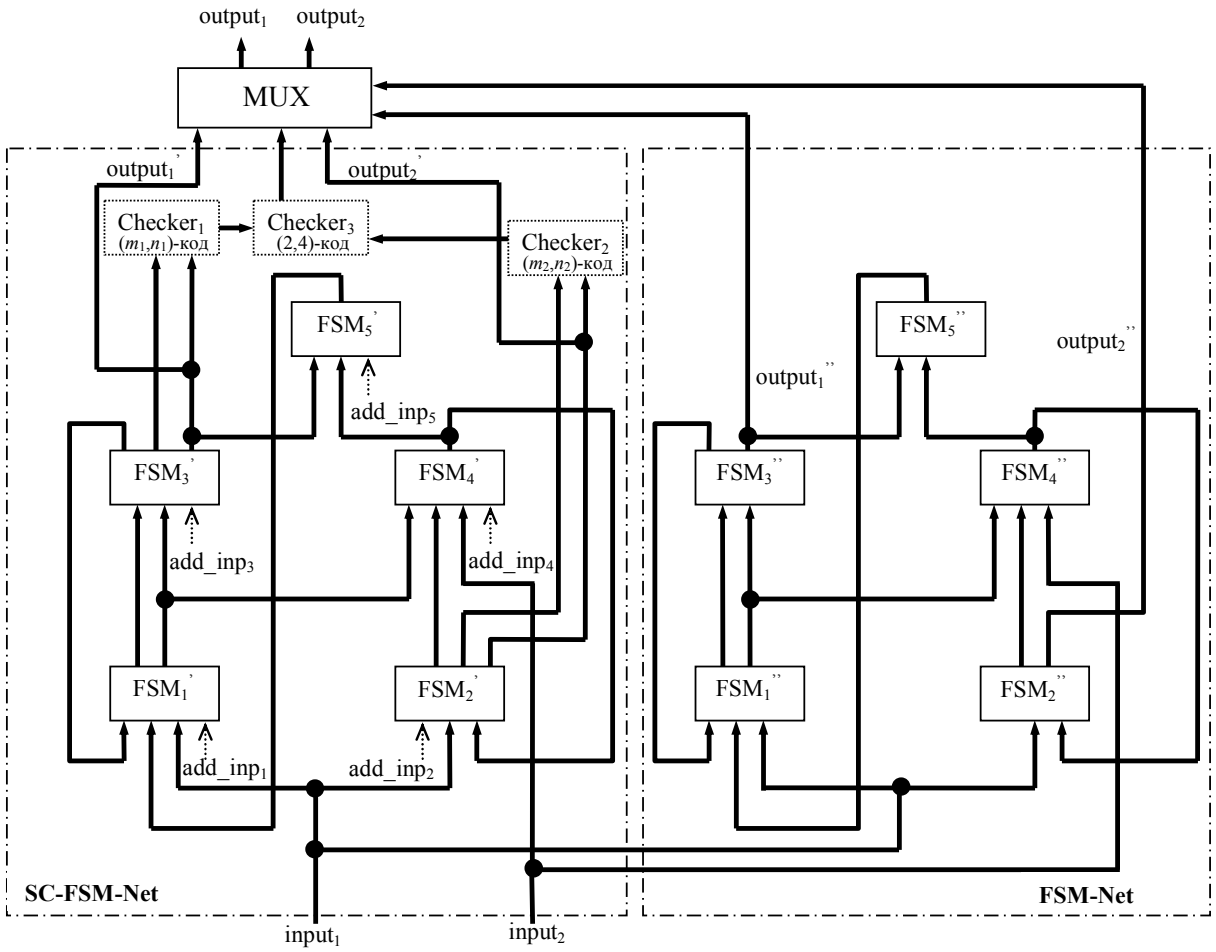

Figure 2. Fault-tolerant synchronous FSM network

(l, $2l$)-code checker (**Checker$_3$**), which transmits the signal about network correctness (malfunction) to the input of the multiplexer.

Each component of the **SC-FSM-Net** network is implemented by a self-checking sequential circuit. A self-checking property is provided for faults at the poles of circuit gates, flip-flops and circuit primary inputs resulting in unidirectional errors at the outputs. The internal states of the FSM are encoded with a constant-weight code. The input states are also encoded by a constant-weight code (or if the input states are already encoded, additional input variables are added in order for the input vectors to become unordered). The output states are encoded in a special way only for those FSMs whose outputs are outputs of network, the constant-weight code or Berger code is used. Further, the structural description of the FSM (obtained after encoding) is minimized by replacing the symbol "0" with "--" in the input cubes. One of the methods which ensures an unidirectional manifestation of stuck-at faults at the outputs of the circuit is used as a method of structural synthesis.

Only one **FSM** in **SC-FSM-Net** can be faulty. Single PDFs for paths that connect an arbitrary input of the combinational part of **FSM$_i$'** to one of its outputs are considered. The occurrence of such faults is limited to one clock cycle. These faults manifest itself as one-bit errors at the output of the combinational part of FSM. The effects of such faults can either disappear without change the correct behavior of the network, or cause unidirectional error at the outputs of the FSM. The unidirectional errors at the outputs of one internal FSM at the next clock cycles can cause the unidirectional errors at the outputs of one or more output FSMs and will be detected by the checkers. Also arbitrary faults of the checkers are allowed, since they do not change the correct functioning of the network.

MUX is a multiplexer that realizes switching of the primary outputs of FSM network (**output$_1$**, **output$_2$**) between the outputs of **FSM-Net** (**output$_1$''**, **output$_2$''**) and the outputs of **SC-FSM-Net** (**output$_1$'**, **output$_2$'**), depending on the values coming from the checker (in Fig. 2 – **Checker$_3$**). The acceptable faults of the multiplexer are faults resulting in an incorrect switching between the outputs of **FSM-Net** and **SC-FSM-Net**. Since these units are fault free and it does not matter where the signal to the network primary output comes from.

4. Conclusion

A method of fault-tolerant FSM network design for path delay faults based on the use of a self-checking FSM network and a FSM network that implements the basic functionality without additional properties was proposed.

This approach allows to reduce hardware overhead due to the fact that in the self-checking FSM network only the output FSMs are observed, which allows reducing the number of checkers, and reduces expenses on the entire fault-tolerant architecture.

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